application; marked up versions of amended claims are attached hereto pursuant to 37 C.F.R. § 1.121(c)(ii). No new matter is involved. Reconsideration and allowance are respectfully requested.

In paragraph 3 on page 2 of the final Office Action, claims 5, and 9 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. The specific reasons are set forth thereafter. In response thereto, Applicant has amended the claims so as to remove the indefiniteness. It is respectfully submitted that these claims and claims dependent therefrom, namely claims 6 and 10-13 are definite and satisfy the requirements of 35 U.S.C. § 112, second paragraph.

In paragraph 6 of the final Office Action, claims 1-4 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 5,661,056 of Takeuchi, Klein et al., Yamada (JP 358106873A) and Wang et al. In paragraph 11, of the final Office Action, claims 7, 8 and 14-18 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Takeuchi. Applicant respectfully traverses these rejections based on the following remarks

The present invention is directed to a non-volatile semiconductor memory cell having a stacked gate structure. A conventional stacked gate structure shown in FIG. 4A includes an insulating layer 2, provided on a p-type silicon substrate 1. The stacked gate structure further includes a floating gate 4 provided through a tunnel insulating layer 3 and an Oxide-Nitride-Oxide (ONO) layer 5 as and inter-layer insulating layer. The inter-layer insulating layer includes a silicon oxide layer

5a, a silicon nitride layer 5b and a silicon oxide layer 5c, respectively. Also, a control gate is provided on the ONO layer 5.

One drawback of the conventional stacked gate structure is the formation of a gap called a "bird's beak" formed between the floating gate 4 and the control gate 6. The bird's break decreases the capacitance coupling between the floating gate 4 and the control gate 6.

One advantage of the present invention is that there is a large capacitance coupling between the control gate and a floating gate while securing an electric field relieving effect and preventing electric charges from leaking. This is accomplished by providing a silicon nitride layer having a low trap density and a low hydrogen density. According to one embodiment of the present invention, a nitride layer is deposited by a Jet Vapor Deposition (JVD) method together with a nitride film deposited by a Chemical Vapor Deposition (CVD) method or an oxide film Thus, the present invention provides for a CVD layer having an typical trap density and a JVD layer having a lower trap density. The cited references fail to disclose this feature.

In terms of particular features according to the invention, a SiN layer formed by a CVD method has a higher hydrogen density than that formed by a LPCVD method, and has a high layer forming rate, as known from the introduction of Wang. Therefore, such a SiN layer obtained by a CVD method is used as a passivation layer or inter-layer insulating layer of portions other than a gate portion, and is not used as a insulating layer of a gate portion (i.e., between a

floating gate and a control gate). This is because a SiN layer obtained by a CVD method is not suitable for a thin layer and for a layer with a low hydrogen density.

As disclosed from the specification of the present application, there are several kinds of ONO layers. One of such layers is an ONO layer comprising a silicon nitride layer formed by the usual LPCVD method, which method is different from the method described in Wang or Klein. The other layer is an ONO layer discussed in Takeuchi. However, such conventional ONO layers are not suitable for an inter-layer insulating layer between a floating gate and a control gate. In other words, it is difficult to form the former ONO layer as a thin, effective layer. The latter ONO layer obtained by a LPCVD method, while including less hydrogen than a layer made by a PECVD method, still includes an appreciable amount of hydrogen. Therefore, if the LPCVD layer contacts the floating gate, various problems such as varying threshold voltage of the transistor occur.

In contrast, the present invention provides the remarkable feature that a silicon nitride layer, such as the layer 15c described, with low hydrogen density and/or low trap density, is used as an inter-layer insulating layer between a floating gate and a control gate, together with layers such as 15b and 15d. Features such as the layer 15c, with low hydrogen density and/or low trap density, are not disclosed by any of the cited references.

In structures according to the present invention, various features are possible. It is possible to make the top oxide layer 15c of the inter-layer insulating layer 15 into a layer which exhibits a low trap density or a low conductivity and

which has a thin conversion thickness. Also, it is possible to suppress an increase of a bird's beak at the post oxidation process without adverse effect by forming a layer which exhibits a low trap density just on the floating gate.

Claims 1-18 are submitted to clearly distinguish patentably over the prior art, taken alone or in the attempted combinations thereof.

In conclusion, the claims as amended herein are submitted to clearly distinguish patentably over the prior art for the reasons set forth above. Therefore, reconsideration and allowance are respectfully requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles telephone number (213) 337-6846 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,

HOGAN & HARTSON L.L.P.

Date: March 8, 2002

By: _____

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**Version with markings to show changes made:**

Rewrite claim 1 as follows:

1. (Twice Amended) A non-volatile semiconductor memory device comprising:

a semiconductor substrate; and

a memory cell having a floating gate provided through a tunnel insulating layer on said semiconductor substrate, and a control gate provided through an inter-layer insulating layer on said floating gate;

wherein said [inter-insulating layer ] inter-layer insulating layer includes:

a silicon oxide layer contiguous to said floating gate;

a first silicon nitride layer provided by a CVD method on said silicon oxide layer; and

a second silicon nitride layer provided by a JVD method on said first silicon nitride layer and having a lower trap density than that of said first silicon nitride layer.

Rewrite claim 2 as follows:

2. (Once Amended) A non volatile semiconductor memory device according to claim 1, wherein said [second silicon nitride layer is formed] JVD method is performed by carrying, over a surface of said substrate, active Si and N

obtained by plasma-decomposing at least a silane series gas and a gas containing nitrogen.

Rewrite claim 5 as follows:

5. (Twice Amended) A non-volatile semiconductor memory device comprising:

a semiconductor substrate; and

a memory cell having a floating gate provided through a tunnel insulating layer on said semiconductor substrate, and a control gate provided through an inter-layer insulating layer on said floating gate,

wherein [silicon nitride layers are formed by a CVD method have a given trap density and said inter-insulating layer said inter-layer insulating layer includes:

a silicon oxide layer contiguous to said floating gate; and

a silicon nitride layer deposited by a JVD method on said silicon oxide layer and having a lower trap density than [that of said given density] an ordinary trap density obtained by a typical CVD condition.

Rewrite claim 6 as follows:

6. (Once Amended) A non-volatile semiconductor memory device according to claim 5, wherein said [silicon oxide layer is deposited] JVD method is performed by carrying, over a surface of said substrate, active Si and N obtained by plasma-decomposing at least a silane-series gas and a gas containing nitrogen.

Rewrite claim 7 as follows:

7. (Twice Amended) A non-volatile semiconductor memory device comprising:

a semiconductor substrate; and

a memory cell having a floating gate provided through a tunnel insulating layer on said semiconductor substrate, and a control gate provided through an inter-layer insulating layer on said floating gate,

wherein said [inter-insulating layer] inter-layer insulating layer includes:

a silicon oxide layer contiguous to said floating gate; and

a silicon nitride layer deposited by a JVD method on said silicon oxide layer and having a quantity of hydrogen content on the order of $10^{19}/cm^3$ or less.

Rewrite claim 8 as follows:

8. (Once Amended) A non-volatile semiconductor memory device according to claim 7, wherein said [silicon nitride layer is deposited] JVD method is

performed by carrying, over a surface of said substrate, active Si and N obtained by plasma-decomposing at least a silane series gas and a gas containing nitrogen.

Rewrite claim 9 as follows:

9. (Twice Amended) A non-volatile semiconductor memory device comprising:

a semiconductor substrate; and

a memory cell having a floating gate provided through a tunnel insulating layer on said semiconductor substrate, and a control gate provided through an inter-layer insulating layer on said floating gate,

wherein [silicon nitride layers are formed by a CVD method have a give trap density and said inter-insulating layer] said inter-layer insulating layer includes:

a silicon nitride layer deposited by a JVD method, serving as a layer contiguous to at least one of said floating gate and said control gate, and having a lower trap density than [that of said given trap density] an ordinary trap density obtained by a typical CVD condition.

Rewrite claim 10 as follows:

10. (Once Amended) A non-volatile semiconductor memory device according to claim 9, wherein said [silicon nitride layer is formed] JVD method is performed by carrying, over a surface of said substrate, active Si and N obtained by plasma-decomposing at least a silane-series gas and a gas containing nitrogen.

Rewrite claim 14 as follow:

14. (Twice Amended) A non-volatile semiconductor memory device comprising:

a semiconductor substrate; and

a memory cell having a floating gate provided through a tunnel insulating layer on said semiconductor substrate, and a control gate provided through an inter-layer insulating layer on said floating gate,

wherein said [inter-insulating layer inter-layer insulating layer includes:

a silicon nitride layer serving as a layer contiguous to at least one of said floating gate and said control gate, and having a quantity of hydrogen content on the order of $10^{19}/cm^3$ or less.

Rewrite claim 15 as follows:

15. (Once Amended) A non-volatile semiconductor memory device according to claim 14, wherein said [silicon nitride layer is formed] JVD method is

performed by carrying, over a surface of said substrate, active Si and N obtained by plasma-decomposing at least a silane-series gas and a gas containing nitrogen